

**REMARKS**

This paper includes a complete and timely response to the final Office Action mailed January 13, 2004 (Paper No. 12). Upon entry of the attached amendments, claims 24-46 remain pending. Claims 1 - 23 were canceled via a previous amendment. Claims 24, 33, 36, and 46 have been amended to clarify the subject matter that the Applicant regards as the invention. The subject matter of amended claims 24, 33, 36, and 46 is included in the circuit embodiments illustrated in FIGs. 3A, 3B, and 4 and described in the corresponding portion of the specification (page 8, line 27 to page 14, line 7). Consequently, no new matter is added.

Each rejection presented in the final Office Action mailed January 13, 2004 is discussed in the remarks that follow.

**I. Claim Rejections Under 35 U.S.C. §102 - Claims 24-46**

**A. Statement of the Rejection**

Claims 24-46 presently stand rejected under 35 U.S.C. §102(b) as allegedly anticipated by *Lesartre et al.* (U.S. Patent No. 5,761,474, hereafter *Lesartre*.)

**B. Discussion of the Rejection - Claims 24 - 46**

Applicant's claims, as amended, are not anticipated for at least the reason that the cited reference fails to disclose, teach, or suggest each element in the claims.

It is axiomatic that “[a]nticipation requires the disclosure in a single prior art reference of *each element* of the claim under consideration.” *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1554, 220 U.S.P.Q. 303, 313 (Fed. Cir. 1983) (*emphasis added*). Therefore, every claimed feature of the claimed invention must be represented in the applied reference (*i.e.*, *Lesartre*) to constitute a proper rejection under 35 U.S.C. §102(b).

**1. Claims 24 - 32**

For convenience of analysis, independent claim 24, as amended, is repeated on the following page in its entirety.

24. A method for finding a predefined plurality of instructions, if available, that are ready to be executed and that reside in an instruction reordering mechanism of a processor that can launch execution of instructions out of order via a predefined number of instruction ports, comprising the steps of:

(a) providing said instruction reordering mechanism having a plurality of said instructions, each said instruction having a respective logic element for causing and preventing launching, when appropriate, of said instruction; and

(b) propagating a set of signals successively through said logic elements of said instruction reordering mechanism, said set of signals responsive to instruction ports and port information, *wherein an instruction identified as valid for launching is launched on an instruction port identified via propagation logic forwarded through said logic elements said propagation logic comprising a next available instruction port identifier when an instruction port is available.*

(Applicant's independent claim 24 - *emphasis added.*)

The cited art of record fails to disclose, teach, or suggest at least the emphasized limitation of pending claim 24 as shown above. Consequently, claim 24 is allowable.

Specifically, the system apparently disclosed in *Lesartre* is arranged such that each instruction slot is dedicated to a particular port. That is, even aqueue slots can only launch to the even port and odd aqueue slots can only launch to the odd port. There are two ports in the aqueue and two ports in the mqueue. So, *Lesartre* propagates information from one instruction slot to the next to indicate whether it's specific port is available for launch. Once a valid operand is identified by *Lesartre* and a corresponding instruction requiring the operand is ready to launch, *Lesartre* launches the instruction to the specified slot and resets the valid operand signal. For *Lesartre*'s implementation with two ports per queue, the even/odd port specific implementation is not too restrictive, but for 4 or more ports, a significant efficiency can be gained by allowing each instruction slot the freedom to launch onto whatever port has not already been taken by older instructions.

In contrast with the system apparently disclosed in *Lesartre* and as claimed in Applicant's independent claim 24, Applicant's method comprises: "propagating a set of signals successively through said logic elements of said instruction reordering mechanism, said set of signals responsive to instruction ports and port information, *wherein an instruction identified as valid for launching is launched on a select instruction port identified via propagation logic forwarded through said logic elements said propagation logic comprising a next available instruction port identifier when an instruction port is available.*

*propagation logic comprising a next available instruction port identifier when an instruction port is available.*" Accordingly, Applicant's claimed method includes port selection in accordance with a next available instruction port identifier, whereas *Lesartre* apparently discloses forwarding an instruction to a specific port of a processor in a one-to-one relationship. Rather than structurally relating each instruction slot to a specified port, Applicant's claimed method launches instructions on a select instruction port identified via propagation logic forwarded through said logic elements of the instruction reordering mechanism. In addition, Applicant's claimed method forwards a next available instruction port identifier when an instruction port is available. Consequently, *Lesartre* does not anticipate Applicant's claim 24. Accordingly, claim 24 is allowable.

Because independent claim 24 is allowable, dependent claims 25-32 are also allowable, as these claims include all the elements of independent claim 24. *See In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988). Accordingly, Applicant respectfully requests that the rejection of claims 24-32 be withdrawn.

## 2. Claims 33 - 35

For convenience of analysis, independent claim 33, as amended, is repeated below in its entirety.

33. A method for quickly finding a predefined plurality of instructions, if available, that are ready to be executed and that reside in a queue of a processor that can launch the execution of instructions out of order, so that the found instructions can be communicated to a corresponding predefined plurality of ports associated with one or more execution resources, comprising the steps of:

(a) providing said queue having a plurality of slots, each said slot for temporarily storing a respective instruction and launching, when appropriate, execution of said respective instruction; and

(b) propagating a set of signals successively through slots of said queue during a launch cycle, said set of signals responsive to available instruction ports and port information to launch execution of an instruction that, when passed through a particular slot:

- (1) select said particular slot for launching when said particular slot is ready by asserting in said slot one or more found signals that identify one or more specific ports associated with said one or more execution resources;
- (2) refrain from selecting said particular slot when said particular slot is not ready by asserting in said slot a lost signal;
- (3) track slots that have been selected during said launch cycle; and
- (4) direct the selection of no more than said predefined plurality of said instructions during said launch cycle,

*wherein an instruction identified as ready for launching is launched on a select instruction port identified via said set of signals forwarded through said queue, said set of signals comprising a next available instruction port identifier when an instruction port is available.*

(Applicant's independent claim 33 - *emphasis added*.)

The cited art of record fails to disclose, teach, or suggest at least the emphasized limitation of pending claim 33 as shown above. Consequently, claim 33 is allowable.

As identified above regarding the patentability of Applicant's independent claim 24, the system apparently disclosed in *Lesartre* is arranged such that each instruction slot is dedicated to a particular port. So, *Lesartre* propagates information from one instruction slot to the next to indicate whether it's specific port is available for launch. Once a valid operand is identified by *Lesartre* and a corresponding instruction requiring the operand is ready to launch, *Lesartre* launches the instruction to the specified slot and resets the valid operand signal.

In contrast with the system apparently disclosed in *Lesartre* and as claimed in Applicant's independent claim 33, Applicant's method comprises: "propagating a set of signals successively through slots of said queue during a launch cycle . . . *wherein an instruction identified as ready for launching is launched on a select instruction port identified via said set of signals forwarded through said queue, said set of signals comprising a next available instruction port identifier when an instruction port is available.*" Accordingly, Applicant's claimed method includes port selection in accordance with a next available instruction port identifier, whereas *Lesartre* apparently discloses forwarding an instruction to a specific port of a processor in a one-to-one relationship. Rather than structurally relating each instruction slot to a specified port,

Applicant's claimed method launches instructions on a select instruction port identified via said set of signals forwarded through said queue. In addition, Applicant's claimed method forwards a next available instruction port identifier when an instruction port is available. Consequently, *Lesartre* does not anticipate Applicant's claim 33. Accordingly, claim 33 is allowable.

Because independent claim 33 is allowable, dependent claims 34 and 35 are also allowable, as these claims include all the elements of independent claim 33. See *In re Fine, supra*. Accordingly, Applicant respectfully requests that the rejection of claims 33-35 be withdrawn.

### 3. Claims 36 - 45

For convenience of analysis, independent claim 36, as amended, is repeated below in its entirety.

36. A system for finding a predefined plurality of instructions, if available, that are ready to be executed in a processor that can launch execution of instructions out of order, comprising:

(a) an instruction reordering mechanism for temporarily storing a plurality of said instructions; and

(b) *a plurality of logic elements associated with said instruction reordering mechanism and associated respectively with each of said instructions in said instruction reordering mechanism for causing and preventing launching, when appropriate, of respective instructions, said logic elements configured to propagate a plurality of signals through said logic elements, said plurality of signals responsive to available instruction ports and port information to launch execution of an instruction identified as valid for launching such that an instruction is launched on an instruction port identified via propagation logic forwarded through said logic elements said propagation logic comprising a next available instruction port identifier when an instruction port is available.*

(Applicant's independent claim 36 - *emphasis added*.)

The cited art of record fails to disclose, teach, or suggest at least the emphasized logic elements of pending claim 36 as shown above. Consequently, claim 36 is allowable.

As identified above regarding the patentability of Applicant's independent claim 24, the system apparently disclosed in *Lesartre* is arranged such that each instruction slot is dedicated to a particular port. So, *Lesartre* propagates information from one instruction slot to the next to indicate whether it's specific port is available for launch. Once a valid operand is identified by *Lesartre* and a corresponding instruction requiring the operand is ready to launch, *Lesartre* launches the instruction to the specified slot and resets the valid operand signal.

In contrast with the system apparently disclosed in *Lesartre* and as claimed in Applicant's independent claim 36, Applicant's system comprises: "*a plurality of logic elements associated with said instruction reordering mechanism . . . said logic elements configured to propagate a plurality of signals through said logic elements, said plurality of signals responsive to available instruction ports and port information to launch execution of an instruction identified as valid for launching such that an instruction is launched on an instruction port identified via propagation logic forwarded through said logic elements said propagation logic comprising a next available instruction port identifier when an instruction port is available.*"

Accordingly, Applicant's claimed system includes logic elements that select one from a plurality of ports in accordance with a next available instruction port identifier, whereas *Lesartre* apparently discloses forwarding an instruction to a specific port of a processor in a one-to-one relationship. Rather than structurally relating each instruction slot to a specified port, Applicant's claimed system launches instructions on an instruction port identified via propagation logic forwarded through said logic elements. In addition, Applicant's claimed propagation logic comprises a next available instruction port identifier when an instruction port is available. Consequently, *Lesartre* does not anticipate Applicant's claim 36. Accordingly, claim 36 is allowable.

Because independent claim 36 is allowable, dependent claims 37-45 are also allowable, as these claims include all the elements of independent claim 36. See *In re Fine, supra*. Accordingly, Applicant respectfully requests that the rejection of claims 36-45 be withdrawn.

4. Claim 46

For convenience of analysis, independent claim 46, as amended, is repeated below in its entirety.

46. A system for finding a predefined plurality of instructions, if available, that are ready to be executed and that reside in a queue of a processor that can launch execution of instructions out of order, comprising:

(a) queue means for storing a plurality of said instructions, said queue means having a plurality of launch logic means for causing and preventing launching, when appropriate, of a respective instruction; and

(b) *logic means associated with said queue, said logic means for propagating a set of signals to successive launch logic means*, said set of signals responsive to available instruction ports and port information to launch execution of an instruction to indicate both when and which of one or more ports of one or more execution resources are available for each said instruction and when none of said ports are available, *wherein an instruction identified as valid for launching by said launch logic means is launched on an instruction port identified via said set of signals forwarded through said launch logic means and wherein said set of signals includes a next available instruction port identifier when an instruction port is available*.

(Applicant's independent claim 46 - *emphasis added*.)

The cited art of record fails to disclose, teach, or suggest at least the emphasized logic means of pending claim 46 as shown above. Consequently, claim 46 is allowable.

As identified above regarding the patentability of Applicant's independent claim 24, the system apparently disclosed in *Lesartre* is arranged such that each instruction slot is dedicated to a particular port. So, *Lesartre* propagates information from one instruction slot to the next to indicate whether it's specific port is available for launch. Once a valid operand is identified by *Lesartre* and a corresponding instruction requiring the operand is ready to launch, *Lesartre* launches the instruction to the specified slot and resets the valid operand signal.

In contrast with the system apparently disclosed in *Lesartre* and as claimed in Applicant's independent claim 46, Applicant's system comprises: "*logic means associated with said queue, said logic means for propagating a set of signals to successive launch means, . . . , wherein an instruction identified as valid for launching by said launch means is launched on an instruction port identified via said set of*

***signals forwarded through said launch means and wherein said set of signals includes a next available instruction port identifier when an instruction port is available.”***

Accordingly, Applicant's claimed system includes logic means for propagating a set of signals to successive launch means wherein an instruction identified as valid for launching is launched on an instruction port identified via said set of signals. In this regard, *Lesartre* apparently discloses forwarding an instruction to a specific port of a processor in a one-to-one relationship. Rather than structurally relating each instruction slot to a specified port, in Applicant's claimed system, “an instruction identified as valid for launching by said launch means is launched on an instruction port identified via said set of signals.” In addition, Applicant's claimed logic means propagates a set of signals that includes a next available instruction port identifier when an instruction port is available. Consequently, *Lesartre* does not anticipate Applicant's claim 46. Accordingly, claim 46 is allowable and the rejection of claim 46 should be withdrawn.

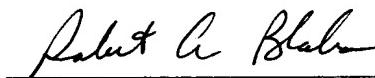
### **CONCLUSION**

In summary, Applicant respectfully requests that all outstanding claim rejections be withdrawn. Applicant respectfully submits that presently pending claims 24-46 are allowable over the cited art of reference and the present application is in condition for allowance. Accordingly, a Notice of Allowance is respectfully solicited. Should the Examiner have any comment regarding the Applicant's response or believe that a teleconference would expedite prosecution of the pending claims, Applicant requests that the Examiner telephone Applicant's undersigned attorney.

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